Education and research at clean room laboratory for silicon device technology at Masaryk University

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Introduction

Masaryk University is operating a clean room laboratory for silicon device technology since April 2007. The laboratory has been designed in partnership with ON Semiconductor Czech Republic. The University covered the construction costs and the company provided guidance during the design and construction of the clean rooms and managed supply, installation and start-up of the technology equipment.

The laboratory aims to **educate** students of physics and microelectronics in a high tech, clean room environment; courses lasting from several ours till 5 days. These dust-free environments are required for the development and manufacture of contamination sensitive silicon-based components. Basic **research** is performed at the new lab as well.

The clean room is equipped by devices covering technology allowing to prepare devices on 100 mm silicon wafers, such as resistors, capacitors, inductors, diodes, transistors.

In school years 2007–2010, students from the Masaryk University, Technical University Brno, Czech Technical University Praha, University Pardubice, University Olomouc and Charles University Praha have passedd 500 courses in the lab. Collaboration with other universities would be welcome.

Acknowledgments

ON Semiconductor (Nasdaq: ONNN) is a leading global supplier of power semiconductor solutions.
ON Semiconductor Czech Republic is located in Rožnov pod Radhoštěm. http://www.onsemi.com

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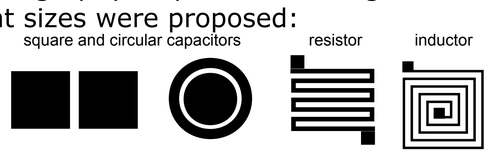
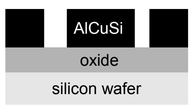
Teaching: Preparation of simple passive devices

Preparation of passive devices is possible by a single photolithography step. The following devices at different sizes were proposed:

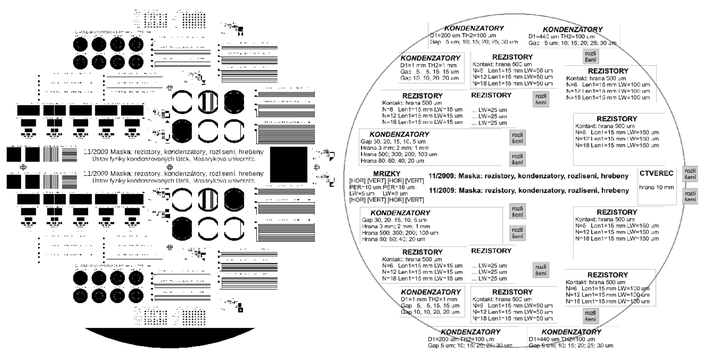


with the following vertical structure:

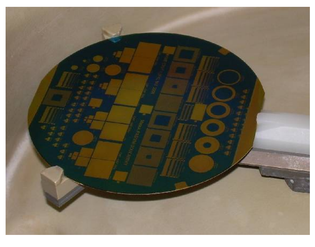


The process flow includes oxidation, sputtering, photolithography, Al etching, photoresist stripping. The process flow is completed by microscopy inspection and measurement of electrical parameters.

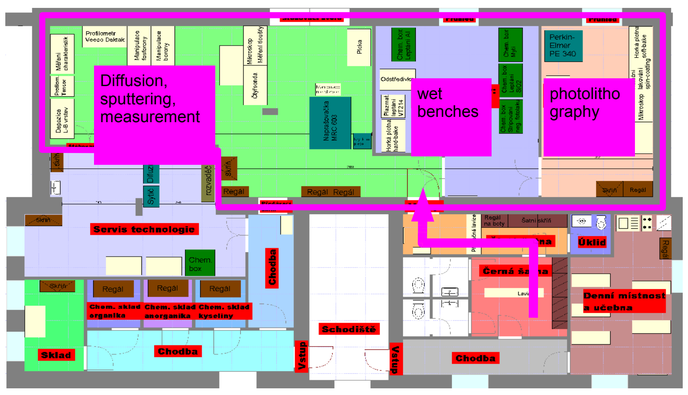
Several masks have been designed, the latest one is below (not to scale – resolution of the photolithography is higher than this poster printer):



Processed wafers:



Clean room facility: 120 m² of clean room area, class 100–1000, i.e. ISO 5–6



Background facilities: 260 m² of support area: service, air conditioning, demineralized water, daily and teaching room, …


Air conditioning


Air supply
Cooling system


Production of DI water: resistivity 18 MΩ·cm @ 25 °C

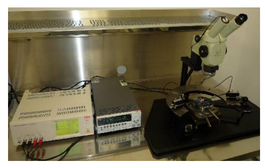
Installed equipment

Oxidation and diffusion
Furnace DA62 with slots for
– Dry oxidation (oxygen)
– Wet oxidation (vapour)
– Boron doping and diffusion
– Phosphorus doping and diffusion

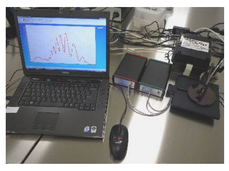
Sputtering of metallization layers
– Sputterer MRC 603,targets AlCuSi and TiW
– Baking at 420 °C

Photolithography
– Perkin-Elmer 340
– Spin coater
– Soft- and hard-bake
– Development

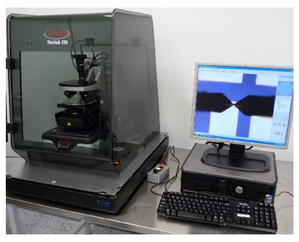
Wet chemical processes
Etching and cleaning
(wet benches)



Plasma stripping in O_2
Device VT214



Thickness measurement
Spectrofotometer, profilometer

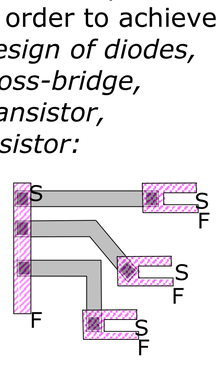


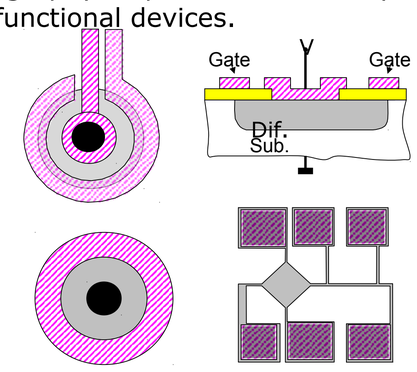
Electric measurements
4pp, characteroscope, AV, LCR

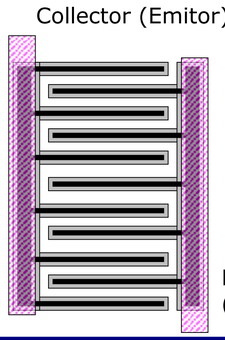
Teaching: Preparation of advanced devices on a chip

An advanced course has been prepared together with the Technical University Brno and Czech Design Center of ON Semiconductor Rožnov pod Radhoštěm. The process needs dopant diffusion and three photolithography steps. It takes six days to complete the process flow procedure in order to achieve functional devices.

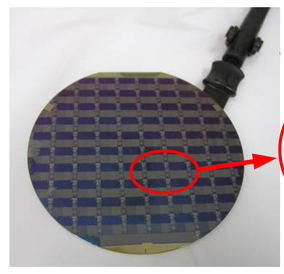
Design of diodes, cross-bridge, transistor, resistor:

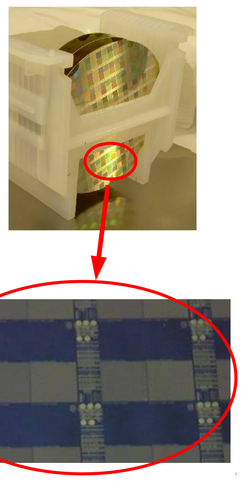






Processed wafers:





Selected research activities

• M. Hovorka, F. Mika, P. Mikulík, and L. Frank, **Profiling N-Type Dopants in Silicon**, Materials Transactions 51 237–242 (2010). Variously doped n-type structures (dopant concentration between 1.5*1016 cm-3 and 1.5*1019 cm-3) on a lightly doped p-type silicon substrate (doped to 1.9*1015 cm-3) have been examined by a photoemission electron microscope equipped with a high-pass energy filter and by an ultra-high vacuum scanning low energy electron microscope. High contrast have been observed between the n-type areas and the p-type substrate and its monotone dependency on the doping level of structures has been manifested. The relation between the energy spectra of photoelectrons and the doping level has been studied, too. The scanning electron microscope images obtained with the landing energy of the primary beam in the low keV range exhibit contrasts similar to those appearing in the full threshold photoemission micrographs.

• P. Kulha, A. Boura, M. Husák, P. Mikulík, M. Kučera, and S. Valenda, **Design and Fabrication of High-Temperature SOI Strain-Gauges**, In proceedings of the 7th International Conference on Advanced Semiconductor Devices and Microsystems ASDAM 2008, 175–178 (2008). The following paper introduces the coventor ware design environment for SOI based piezoresistive sensor design. Fabrication process and characterization of designed sensors is also presented. The software package Coventor Ware has been used for design of mechanical and electrical characteristics of the structure. The tools enable design, modelling and successive modification of designed MEMS structures. The program enables: drawing of 2D layout and its editing, simulation of production process, generation of 3D model from 2D masks, generation of network by the method offinite elements, solution of mechanical, piezoresistive, thermal and further simulations. Simple passive elements (strain sensitive resistors - piezoresistors) were fabricated on SIMOX SOI substrates with sputtered AlCuSi metallization. Basic parameter extraction and their temperature dependence were performed.

• F. Kadlec, P. Kužel, P. Mikulík, et al. **Actively tunable structures and metamaterials for the terahertz range**. Design and development of structures and devices for the terahertz range.

• M. Meduňa, O. Caha, J. Kuběna, P. Mikulík, et al. **Nucleation and growth of oxygen precipitates in silicon**. Study of nucleation processes in silicon wafers.

Laboratory leaflet

Conclusion

New university clean room laboratory for silicon device technology has been established. The laboratory is devoted to **education** and **research** and it is the only such facility in the Czech Republic. Masaryk University welcomes collaboration with other Czech and foreign universities and research institutions and companies. Such collaboration has been already started: teaching students from other universities, research projects with researchers from institutes of the Academy of Sciences.